Remarks

Claims 1 and 4-39 are pending in the application.

Claims 1, 4-27, and 31-39 have been allowed.

Claims 28 and 29 are rejected.

Claim 30 is objected to.

Allowable Subject Matter

Claims 1, 4-27, and 31-39 have been allowed. The Applicant thanks the Examiner for acknowledging the patentable subject matter of these claims. Claim 30 has been objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The Applicant also thanks Examiner for acknowledging the allowability of claim 30; however, for reasons mentioned below, the Applicant submits that claim 28 is in proper form for allowance and hence claim 30, which depends from claim 28, is likewise in proper form for allowance.

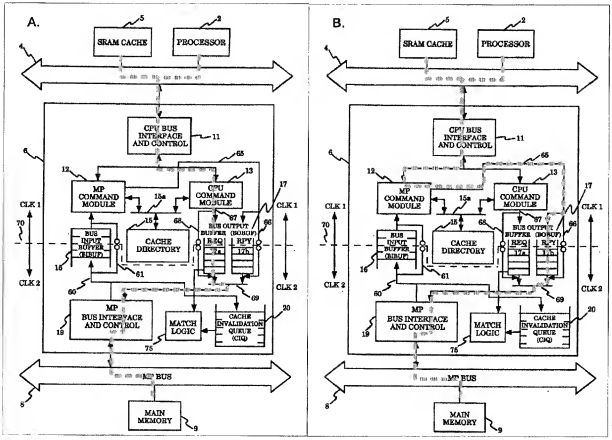
Claim Rejection – 35 U.S.C. § 102

Claims 28 and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Chang et al. (U.S. Patent No. 5,398,325). The Applicant respectfully traverses the rejection.

Claim 28 stands rejected under § 102(b) as anticipated by Chang. Claim 28 recites an article of manufacture comprising computer-readable media containing instructions that, when executed by a processor, cause that processor to perform a method comprising: transmitting commands over a system management bus to a first buffered memory module to cause that buffered memory module to exercise a memory channel between the first buffered memory module and a second buffered memory module; and receiving results of the transmitted commands from the first buffered memory module over the system management bus.

In contrast, Chang fails to teaeh this limitation. Specifically, Chang teaches a "single copy cache tag cache memory structure . . . wherein said first buffer means further comprises a local data bus coupled to receive said request and reply commands buffered by said first and second buffers, said local data bus further coupled to said second bus commands to said computer devices operating on said second bus, including said main memory." Col. 10, Lines 39-47. If the first and second buffers taught in Chang are the first and second buffered memory

modules, then the first buffered memory module is not caused to exercise a memory channel between the first buffered memory module and the second buffered memory module as recited in claim 28. For example, consider the following figures A and B, each of which generally corresponds with Figure 2 of Chang. Please note that the Applicant has added thick dotted gray lines to illustrate a point.

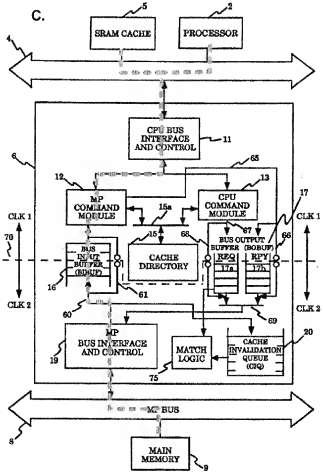


As shown in these figures, and corresponding teachings of the Chang specification, Chang fails to teach that a memory channel is exercised between buffer structure 17a and buffer structure 17b. The flow of information, as taught by Chang, passes through each of the individual buffer structures, but does not pass between them. In Figures A and B above, the dotted gray lines show the interconnections which guide the data communications between devices coupled to the CPU bus 4 and devices coupled to the MP bus 8. Col. 5, Lines 17-27 and Col. 5, Lines 31-47. Thus, a first buffered memory module does not cause that buffered memory

module to exercise a memory channel between the first buffered memory module and a second buffered memory module, as taught in claim 28.

Similarly, consider the following Figure C which also corresponds generally with Figure 2 of Chang:

C.



Chang also fails to teach that a memory channel is exercised between buffer structure 16 and buffer structure 17. Chang teaches that "[b]uffers 16 and 17 enable communieations between devices operating on CPU bus 4 and devices operating on MP bus 8" Col. 6, Lines 6-8. In Figures C above, the dotted gray line shows the interconnections which guide the data communications through buffer 16 and between devices coupled to the CPU bus 4 and devices coupled to the MP bus 8. In other words, Chang does not teach that a memory channel is exercised between a first buffered memory module and a second buffered memory module. Irrespective of whether 16, 17a, or 17b are chosen as the alleged memory buffered memory

modules of claim 28, a memory channel is not exercised between any them. Thus, the Applicant submits that claim 28 is in allowable form.

Further, the Examiner suggests that a cache arrangement 5 of Figure 2 is the computer-readable media of claim 28, and an instruction sought in the cache arrangement 5 is the instructions that, when executed by a processor, cause that processor to perform the method of claim 28. However, it is not clear—nor is it taught—in the Chang specification that instructions stored in the cache arrangement 5 control the operation of buffer structures in the cache controller 6, much less causing a processor to exercise a memory channel between a first buffered memory module and a second buffered memory module. *See* Figure 2 and Col 7., Lines 43-46. Thus, claim 28 is in proper form for allowance.

Claims 29 and 30 depend from claim 28. Based at least on this dependency, claims 29 and 30 are consequently also allowable.

For the foregoing reasons, reconsideration and allowance of claims 28-30 of the application is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Dated: September 13, 2006

Respectfully submitted,

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